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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,457	04/27/2006	Takamitsu Yamanaka	AI 409NP	5045

23995 7590 01/26/2010

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EXAMINER	
CHHAYA, SWAPNEEL	
ART UNIT	PAPER NUMBER
2895	

MAIL DATE	DELIVERY MODE
01/26/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,457	YAMANAKA, TAKAMITSU	
	Examiner	Art Unit	
	SWAPNEEL CHHAYA	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/26/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *4-17* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshihiro (JP 06-268162). In view of Jeng et. al. (U.S. Patent 6136643)

1. Yoshihiro discloses:

A semiconductor device comprising:

a semiconductor substrate (Fig. 1 10 page 2 paragraph 0013)

a first region defined on the semiconductor substrate and having a first device formation region isolated by a device isolation portion formed by filling an insulator in a trench (33) formed in the semiconductor substrate; (Fig. 1 page 2 paragraphs 0013-0016)

a first device (30) provided in the first device formation region (Fig. 1 page 2 paragraph 0014-0015)

a second region (33) defined on the semiconductor substrate separately from the first

region and having a second device formation region (Fig. 1 page 2 paragraph 0014)

and

a second device provided in the second device formation region and having a higher breakdown voltage than the first device, the second device having a drift drain structure in which a LOCOS oxide film thicker than a gate insulation film thereof is disposed at an edge of a gate electrode thereof. (Fig. 1-2 page 2 paragraph 0014-0015), please note that the drift drain structure is defined in the specification of the applicant wherein the concentration of the electric field is prevented by locating the thick oxide film at the edge of the gate electrode

the insulator of the device isolation portion and the locos oxide film are continuous at a boundary between the first region and the second region (Fig. 1)

Jeng discloses:

Wherein a surface of the device isolation portion and a surface of the semiconductor substrate are both arranged in a common plane (column 2 lines 35-46)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to create the STI that is planar with the substrate surface as taught by Jeng, since Jeng states at column 2 lines 35-46 that such a modification would electrically isolate each device area in and on the substrate.

2.

A semiconductor device as set forth in claim 1,

wherein the second device formation region is a region isolated by a device isolation portion formed by filling an insulator in a trench formed in the semiconductor substrate. (Fig. 1 page 2 paragraphs 0013-0016)

3.

A semiconductor device as set forth in claim 1,

wherein the second device formation region is a region isolated by a LOCOS oxide film. (Fig. 1-2 page 2 paragraph 0014-0015),

4.

A semiconductor device as set forth in claim 1, wherein the first device has a smaller device size than the second device. (Fig.1)

Response to Arguments

1. Applicant's arguments filed 9/24/2009 have been fully considered but they are not persuasive.

2. Applicant has argued: "The Examiner's Action mailed on June 24, 2009, has been received and its contents carefully considered. It is respectfully requested that this Amendment be entered after final rejection under 37 CFR §1.116(b) (2) as placing the application in better form for consideration on appeal.

In this Amendment, Applicant has amended claim 1. Claim 1 is the sole independent claim pending and under consideration, and claims 1, 2 and 4 remain pending and under consideration in the application, claims 3 and 5-17 having been previously withdrawn in response to the Restriction Requirement of November 3, 2008, although claim 3 has been deemed by the Examiner to be directed merely to a different species of the elected invention, and is thus subject to possible rejoinder. For at least the

following reasons, it is submitted that this application is in condition for allowance.

Claims 1-4 were rejected under 35 USC §103(a) as obvious over the combination of Hirota (JP 06-268162 A) in view of Jeng et aL (US 6,136,643). Please note that the Office Action refers to the primary reference as Yoshihiro, but this appears to be a given name, and Hirota the surname. This rejection is respectfully traversed.

Hirota discloses a semiconductor device having an ordinary-breakdown- strength MOS transistor 30 and a high-breakdown-strength MOS transistor 11 both formed on a semiconductor substrate 10. However, a LOCOS isolation

structure using a field oxide film 33 is applied to both the regions around the ordinary-breakdown-strength MOS transistor 30 and around the high-breakdown- strength MOS transistor 11.

According to the present invention, on the other hand, an STI (Shallow Trench Isolation) structure is adopted for the first region including the device with the lower breakdown voltage, while a LOCOS structure is adopted for the second region including the device having the higher breakdown voltage. Thus, the present invention is structurally different from Hirota. See the present specification as filed, e.g. [0036] and [0069]:

[0001] With this arrangement, so-called shallow trench isolation (STI) is employed for the device isolation in the first region formed with the first device of the lower breakdown voltage, so that the microminiaturization of the structure in the first region can be advantageously achieved. On the other hand, the second device of the higher breakdown voltage formed in the second region has the drift drain structure with the LOCOS oxide film provided at the edge of the gate electrode, so that the problem of the concentration of the electric field can be suppressed which may otherwise occur when a thick insulation film of an STI portion is disposed on the edge of the gate electrode. Thus, the second device has a sufficient breakdown voltage.

[0002] The lower breakdown voltage transistors 51 formed in the first region 50 are respectively disposed in device formation regions 53 isolated by a shallow trench isolation (STI) portion 52 formed in a surface of the silicon substrate 40. The STI portion 52 is formed by filling silicon oxide 55 in a shallow trench 54

(e.g., having a depth of about 4000A) formed in the surface of the semiconductor substrate 40.
In the STI portion of the structure of the present invention, the surface of the device isolation portion and the surface of the semiconductor substrate are flush with each other, i.e., the surfaces are in the same plane.

3. The structure of the device according to Hirota is shown in Drawing 1 thereof, from which it is apparent that the field oxide film 33 is not flush with a surface of the substrate, but instead stands proud therefrom, i.e. the field oxide film 33 does not have a surface in a common plane with a surface of the substrate. This follows directly because the field oxide film 33 has been made by local oxidation, i.e. by a LOCOS process, and not by filling a trench,' whereas in the present invention the device isolation portion is made by filling a trench until it is flush with the substrate:
Hirota (Yoshihiro) thus fails to disclose a structure in which an STI structure is adopted for a first region while a LOCOS structure is adopted for a second region.
The Office Action states on page 3 thereof that Jeng et aL discloses "Wherein a surface of the device isolation portion and a surface of the semiconductor substrate are both arranged in a common plane" in column 2, lines 35-46 thereof:
... This allows self-aligned contacts to be made with relaxed photolithographic alignment tolerances.
The method begins by providing a semiconductor substrate. Typically. the substrate is a P doped single-crystal silicon substrate having a 100> crystallographic orientation. Device areas are provided by forming a relatively thick Field Oxide (FOX) that surrounds and electrically isolates each device area in and on the substrate. One method of forming the field oxide is by shallow trench isolation (STI) in which a shallow trench is etched in the substrate and filled with a silicon oxide (SiO2) that is made essentially planar with the substrate surface.

Thus, Jeng et aL discloses an STI structure. However, Jeng et al. fails to teach or suggest a structure that includes within it both an STI structure and a LOCOS structure.
As Hirota (Yoshihiro) and Jeng et al. both fail to teach or suggest a structure that includes an STI

structure in a first region and a LOCOS structure in a second region, they must naturally fail to teach or suggest a structure in which an insulator for the STI structure is continuous with a LOCOS oxide film at a boundary between the first and second regions.

That is to say, neither Hirota (Yoshihiro) nor Jeng et aL, whether taken separately or in combination, teaches or suggests "wherein the insulator of the device isolation portion and the LOCOS oxide film are continuous at a boundary between the first region and the second region" as recited in claim 1.

Consequently, claim 1 patentably defines over Hirota (Yoshihiro) and Jeng et al. and is allowable, together with claims 2 and 4 dependent therefrom, and as claim 1 is generic it is respectfully requested that the species of withdrawn claim 3 be rejoined with the species of claims 2 and 4, and claim 3 allowed therewith.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No remittance is believed to be due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly. “

Regarding the amendment, the drawing of Hirota clearly shows the oxide film (33) being continuous. Furthermore, with regards to applicant's argument that Jeng and/or Hirota fail to disclose both an STI as well as a LOCOS structure, this is the response to Applicant’s piecemeal analysis of the references, it has been held that one cannot show nonobviousness by attacking references individually where, as here, the rejections are based on combinations of references. In re Keller, 208 USPQ 871 (CCPA 1981).

Conclusion

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SC

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895